## AMENDMENTS TO THE CLAIMS

**This listing of claims will replace all prior versions and listings of claims in the application:**

## LISTING OF CLAIMS:

1. (currently amended): A deinterleaving apparatus for a digital communication system, comprising:

a row counter which~~for~~ increase~~sing~~ a row counting value for a row period based on input data;

a column counter which~~for~~ increase~~sing~~ a column counting value for a column period for each row counting value~~in every row period~~ set in the row counter;

plural row synchronous counters each corresponding to a different~~the~~ row counting value~~period~~, and ~~for~~which each increase~~ing~~ a synchronous counting value corresponding to the row counting value through~~in~~ each~~every~~ column period set in the column counter;

an offset memory which~~for~~ store~~sing~~ offset values set in correspondence to interleaving delay depths of the input data for each channel; and

a deinterleaver memory which~~for~~ store~~sing~~ the input data at a write address generated based on the offset values, wherein the input data stored in the deinterleaver memory is read at a read address generated based on the synchronous counting value.

2. (currently amended): The deinterleaving apparatus as claimed in claim 1, wherein the plural row synchronous counters each have a different synchronous period from each other ~~in correspondence to the row counting value~~.

3. (original): The deinterleaving apparatus as claimed in claim 1, wherein a column period set in the column counter corresponds to a synchronous signal of the digital communication system.

4. (currently amended): The deinterleaving apparatus as claimed in claim 1, wherein the input data includes valid and invalid data depending upon interleaving delay depths for each channel, and the valid data is read at the read address generated based on the synchronous counting value corresponding to the row counting value.

5. (currently amended): The deinterleaving apparatus as claimed in claim 1, wherein the read and write addresses are generated based on ~~in combination of~~ the row counting value, the column counting value, and the synchronous counting value corresponding to the row counting value.

6. (currently amended): The deinterleaving apparatus as claimed in claim 1, wherein the write address is generated based on a sum of the column counting value and ~~to which~~ the offset value ~~is added~~, and the synchronous counting value corresponding to the row counting value.

7. (original): The deinterleaving apparatus as claimed in claim 1, further comprising plural multiplexers for selectively switching, so as to output a signal for writing and reading with respect to the deinterleaver memory.

8. (currently amended): A deinterleaving method for a digital communication system, comprising steps of:

increasing a row counting value of a row counter based on input data;

increasing a column counting value of a column counter for~~every~~ each row counting value~~period~~ set in the row counter;

increasing synchronous counting values of each of plural row synchronous counters through every column period set in the column counter;

storing in a deinterleaver memory the input data at a write address generated based on offset values set in correspondence to interleaving delay depths of the input data for each channel; and

reading the input data stored in the deinterleaver memory at a read address generated based on the synchronous counting values,

wherein each plural row synchronous counter corresponds to a different row counting value..

9. (currently amended): The deinterleaving method as claimed in claim 8, wherein the plural row synchronous counters each have a different synchronous period from each other ~~in correspondence to the row counting value~~.

10. (original): The deinterleaving method as claimed in claim 8, wherein a column period set in the column counter corresponds to a synchronous signal of the digital communication system.

11. (currently amended): The deinterleaving method as claimed in claim 8, wherein the input data includes valid and invalid data depending upon interleaving delay depths for each channel, and, in the data-reading step, the valid data is read for an output at the read address generated based on the synchronous counting value corresponding to the row counting value.

12. (currently amended): The deinterleaving method as claimed in claim 8, wherein the read and write addresses are based on ~~generated in combination of~~ the row counting value, the column counting value, and the synchronous counting value corresponding to the row counting value.

13. (currently amended): The deinterleaving method as claimed in claim 8, wherein the write address is generated based on a sum of the column counting value and ~~to which~~ the offset value ~~is added~~, and the synchronous counting value corresponding to the row counting value.

14. (original): The deinterleaving method as claimed in claim 8, wherein each step further includes a step for selectively outputting a signal with respect to a predetermined input signal.